## ABSTRACT OF THE DISCLOSURE

A digital arithmetic operation circuit includes a plurality of arithmetic operation blocks, a control signal generator and a selector. The plurality of arithmetic operation blocks receive a plurality of digital input signals and perform different arithmetic operations on the received digital input signals, in parallel, to output operation result signals. The a control signal generator receives a plurality of digital input signals and generates a control signal based on the digital input signals. The selector selects one of the operation result signals, in response to the control signal, to output the selected operation result signal. After the control signal generator supplies the control signal to the selector, the selector outputs the selected operation result signal as soon as the selected operation result signal is supplied to the selector.